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BRL

GUN DISPLAY UNIT HARDWARE INTERFACE: FIREPOWER CONTROL EXPERIMENT PART 9 OF 12

MARK D. KREGEL

SEPTEMBER 1990

U.S. ARMY LABORATORY COMMAND

BALLISTIC RESEARCH LABORATORY
ABERDEEN PROVING GROUND, MARYLAND

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From 2 through 20 December 1985, the U.S. Army Ballistic Research Laboratory, in cooperation with the U.S. Human Engineering Laboratory, conducted a Firepower Control Experiment. Among other things, this experiment collected information on the communications among the various players who represented the elements of fire direction and support. These elements included fire direction officers, field artillery battery fire direction centers, battery computer systems, and simulated 155-mm howitzer firing units. The purpose of this report is to describe the author's design and his construction of the electronic interface device which allowed commercial computers to intercept messages received over the military communications channels used during the experiment as well as allowing these computers to inject messages over those same communications channels.

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PREFACE

This is one of a series of reports that covers the U.S. Army Ballistic Research Laboratory's (BRL's) Firepower Control Experiment conducted during the period 2-20 December 1985 at the jointly developed BRL and U.S. Army Human Engineering Laboratory (HEL) Command Post Exercise Research Facility (CPXRF). A total of twelve reports will be published, and each covers a specific topic.

This report is part 9 of 12; a complete list of these reports with associated authors follows.

TITLE	AUTHORS
Concept and Purpose Firepower Control Experiment Part 1 of 12	Samuel C. Chamberlain
Ether & Bit Box Programs Firepower Control Experiment Part 2 of 12	George W. Hartwig
ADIS Program Firepower Control Experiment Part 3 of 12	Virginia A. Kaste
MFOSCE Program Firepower Control Experiment Part 4 of 12	Louise D. Kokinakis
Software Library for *Ether, ADIS, & MFOSCE Programs* Firepower Control Experiment Part 5 of 12	Virginia A. Kaste, George W. Hartwig, and Louise D. Kokinakis
The Enhanced Fire Direction Simulator Firepower Control Experiment Part 6 of 12	Douglas C. Brodeen and Thomas A. DiGiacinto

1. INTRODUCTION

From 2 December through 20 December 1985, the U.S. Army Ballistic Research Laboratory (BRL), in cooperation with the U.S. Human Engineering Laboratory (HEL), conducted a Firepower Control Experiment. Among other things, this experiment collected information on the communications among the various players who represented the elements of fire direction and support. These elements included fire direction officers, field artillery battery fire direction centers, battery computer systems, and simulated 155-mm howitzer firing units. In addition to the representatives of the BRL and the HEL, there were also representatives from the U.S. Army Field Artillery School, Fort Sill, Oklahoma.

The purpose of the experiment was to develop "rules of thumb" for the fire direction officer that would be useful in selecting the type and volume of ammunition in various possible engagements. During the experiment, various items of military equipment were used such as Gun Display Units (GDUs), radios and other communication links, field battery computers, computer graphics displays, and input or control devices. In addition, commercial computers were used to monitor and, at times, to participate in the exercise.

Since it was necessary to "shift" through the various communications between the players or elements to gain insight into the strategies of each, a means had to be found to convert the "military" analog radio communications in real time into serial binary communications that could be recorded and processed on the commercial computers. Also, in order to simulate military equipment impractical to use in the experiment, such as weapons, the commercial computers either simulated such equipment in real-time or allowed player input through the computers. This necessitated the use of a link from the commercial computers, through the RS232 standard serial interface, to the military form of radio communications that consisted of analog tones. Such a link was designed and constructed by the author for use during the Firepower Control Experiment.

The purpose of this report is to describe the author's design and his construction of this link, or electronic interface device, which allowed the commercial computers to intercept messages received over military communications channels, as well as allowing these computers to inject messages over those same communications channels; that is, to describe a device that will allow the monitoring of military communications and the transforming of such communications from analog "tones" of various frequencies and durations into a serial digital form compatible with commercial computers and the reverse, conversion

of serial digital communications into tones capable of being transmitted over military communication links as analog signals. This device will be referred to as the gun display unit-commercial computer interface board, or simply as the interface board.

2. CIRCUIT DESCRIPTION

In operation, the interface board provides two basic functions. The first function is to provide an interface between radio analog communications and RS232 compatible serial communications that feed into commercial computers. This function is referred to as "demodulation." The second function is to provide an interface between RS232 compatible serial communications and radio analog communications as used by the military. This function is termed "modulation" and is just the reverse of the first one. One may think of radio communications as audible tones that, when played through a speaker, can be discerned in terms of the tones present. The RS232 serial communications, on the other hand, denotes a changing voltage that can have only one of two possible values, a positive value and a negative value. Because of their nature, RS232 level signals cannot be transmitted over a radio, but must be converted into an analog form of communications if radio communications are desired.

The radio analog communications consists of a single channel of audio information. At any one instance during which the channel is active there is either a 1,200-Hz tone or a 2,400-Hz tone being transmitted and is considered to be of the form of an oscillating electrical voltage. Each tone lasts for a period of one and two thirds milliseconds. This period of time allows for the transmission of exactly two 1,200-Hz tone cycles or four 2,400-Hz tone cycles. Each tone cycle is in the form of a cosine function, defined over the interval of zero to two pi radians. The transmission of four consecutive 2,400-Hz tones corresponds to a positive logic level at the output of the demodulator of the interface board. The transmission of two 1,200-Hz tones corresponds to a negative logic level at the output.

Since two 1,200-Hz tone cycles or four 2,400-Hz tone cycles are used to define the logic of each bit transmitted or received, the bit rate for the modulation and demodulation must be 600 bits per second. Some bits transmitted in a message are synchronization bits and the rest are data bits according to the communication standard used by the GDU. The interface board described herein does not manipulate the bits in terms of message content but only converts the bit information from one format to another.

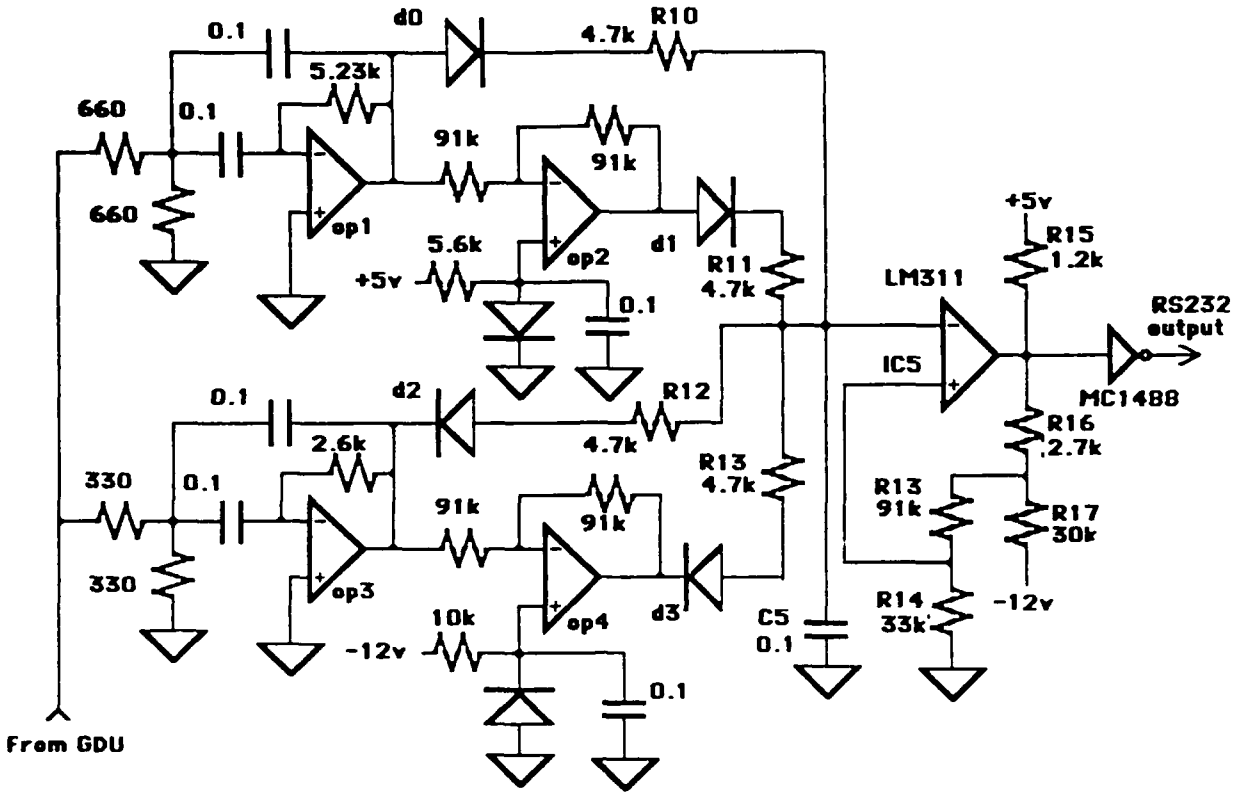

Figure 1. Schematic Diagram of the Demodulator Section of the Interface Board.

The RS232 standard allows two-way or full-duplex communications. As a consequence, the output of the MC1488 quad-line driver in Figure 1 can always be active. When the interface board is not sending information over the RS232 link it maintains the line in a "marking" state. The GDU communications, on the other hand, allows only one message at a time to flow between the interface board and the GDU because of interference on a single radio channel. That is, the interface board has, in effect, an open channel (two-way communications) for its RS232 output, linking it to the civilian computer. Any transmission to the computer will not interfere with messages received at the same time from the computer.

Other types of designs or changes in component values for the present design are possible. Since then, Waddell (1987), a summer student associated with the DoD Science and Engineering Apprenticeship Program, used numerical techniques to analyze the design of the demodulator as well as to optimize component values for the case of degraded waveforms. His analysis yielded somewhat different resistor and capacitor values from that shown in Figure 1 and suggested a potential for improved performance. Though his results have not been implemented in hardware, users that might have similar requirements for an inexpensive interface board should consider his results.

A schematic diagram of Waddell's demodulator circuit, which is a variation of the one of Figure 1 with the inclusion of two signal conditioning filters, is shown in Figure 2. By establishing a criterian of performance in the presence of degraded input waveforms, Waddell was able to optimize component values numerically by writing a computer simulation of the actual circuit using advanced numerical techniques.

The integrated circuits in this figure serve the same function as in Figure 1.

4. MODULATOR SECTION OF THE INTERFACE BOARD

The function of the modulator is far simplifier than that of the demodulator. Basically, all the modulator does is generate either a 1,200-Hz signal or a 2,400-Hz signal for transmission through a radio from information received from an RS232 interface. In addition, the modulator must activate a relay during times of transmission, which is equivalent to "keying" a microphone to talk.

The modulator section consists of three elements. The first is a logic element used to detect transitions in the input and to select the output frequency, the second is a retriggerable mononstable multivibrator element driving a relay, and the third element is a cosine function analog output generator. In operation the logic element determines the frequency of the cosine function to be generated by the cosine analog output generator. The logic element also provides information on transitions in the input logic level to the multivibrator element that allows the multivibrator to hold the relay in a "transmit" state as long as new data is being presented to the input.

A schematic diagram of the modulator section of the interface board in shown in Figure 3.

The modulator section also consists of an RS232 to TTL logic level converter, a system clock input, a divide-by-64 circuit, and associated logic that interfaces these elements.

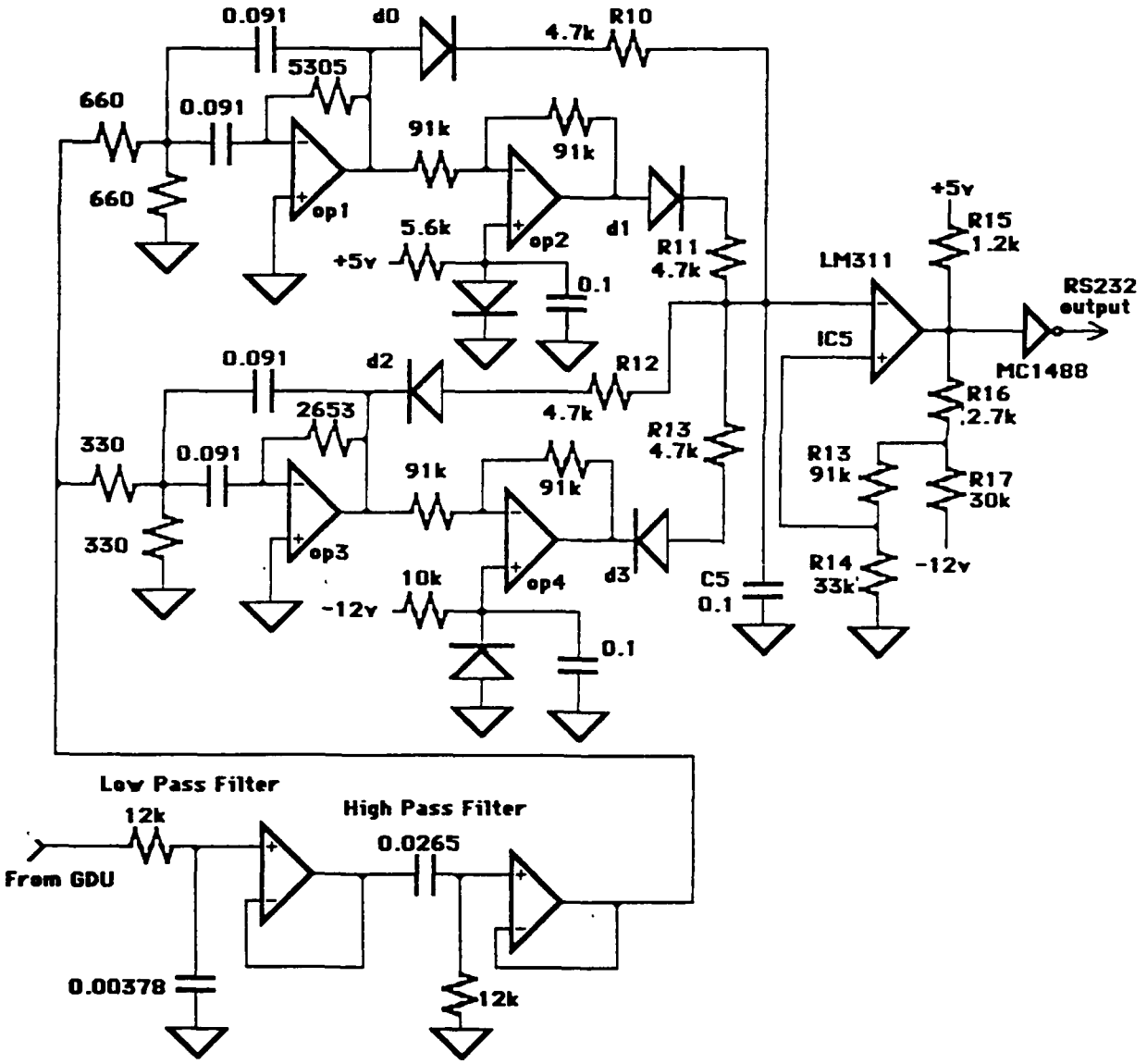

Figure 2. Schematic Diagram of the Revised Demodulator Section of the Interface Board Due to Waddell (1987).

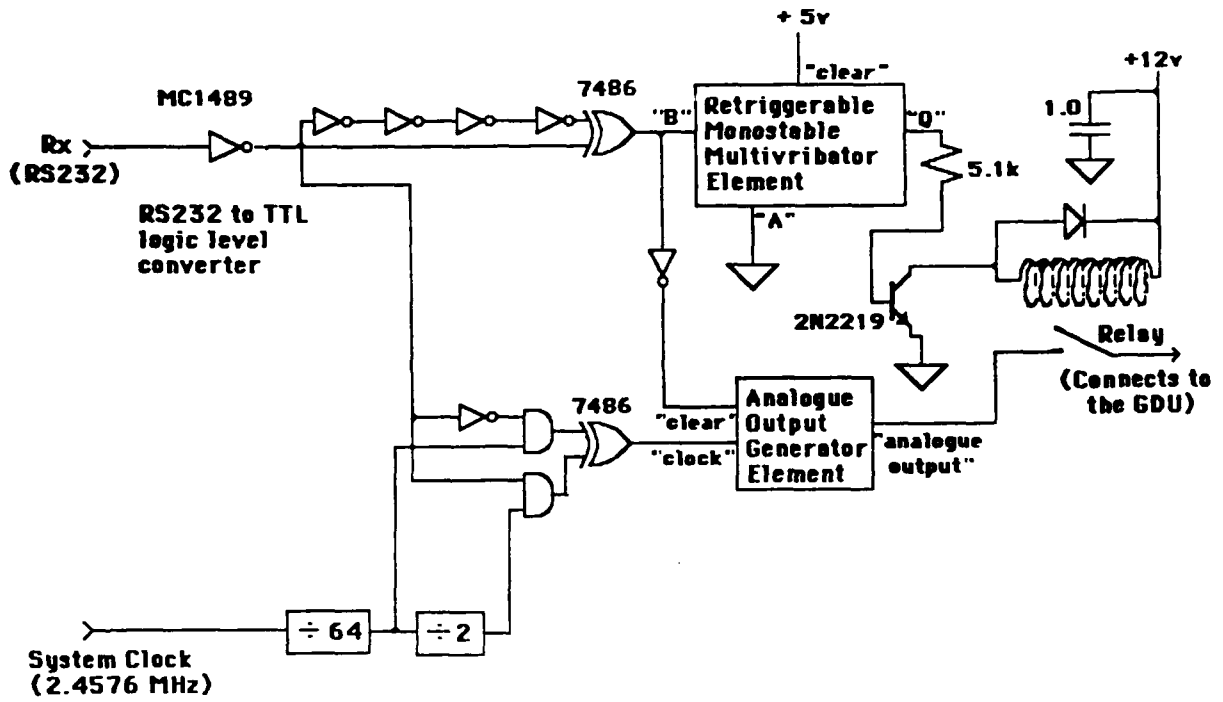

Figure 3. Schematic Diagram of the Modulator Section of the Interface Board and Its Various Elements.

Input to the modulator consists of a signal from the RS232 serial communications line that connects the receive (Rx) portion of the interface board to the commercial computer. Since RS232 signals are incompatible with transistor-to-transistor logic used on the interface board, one section of a MC1489 quad-line receiver integrated circuit is used to convert the RS232 logic level signal to a TTL logic level signal.

Transitions in the input are used to hold the relay in a closed position connecting the cosine analog output generator to the GDU Transmit (Tx) line. Transitions are detected by one section of a 7486 quad 2-input exclusive-or gate integrated circuit. If the two inputs of the 7486 IC are of opposite logic levels, the output will be false (or logic level 0). If they are opposite, then the output will be true (or logic level 1). Thus, if input to one of the two inputs is delayed, then a positive going transition (true) will be generated whose width in time is equal to the time of the delay. This will occur on every transition received from the MC1489 logic level converter regardless whether it is a low to high transition or a high to low transition. The delay is generated by four TTL inverters as shown in Figure 3.

These short positive pulses that arise on either positive or negative transitions of the input are fed to the input of one section of a 74123 retriggerable monostable multivibrator integrated circuit.

The 74123 retriggerable monostable multivibrator is programmed by a resistor capacitor circuit to have a positive output pulse at Q of a specific width. As long as an input pulse occurs within the time the output of the multivibrator is positive, the multivibrator will remain in its set (true) state, but its period will be extended. A diagram of the 74123 triggerable monostable multivibrator with "clear" is shown in Figure 4 along with the timing resistor and capacitor.

In addition to the 74123 retriggerable monostable multivibrator IC, this figure also shows the external resistor and capacitor used in programming the output pulse width. Input is to "B" with "A" set to ground. The "clear" input is set to high. Output is from "Q."

Note that in the interface board only the right section of the 74123 is used. The left section is left unconnected. Input to the element is at "B" of the right section of the 74123 IC with the corresponding input "A" set low and "clear" set high.

This output pulse width is normally made to be many tens-of-bit-widths in duration or length, perhaps as long as 20 msec. The duration of the pulse width is controlled by R40 and C40, as shown in Figure 4. The values shown in Figure 4 give a nominal delay of 14 msec. Exact values of this delay are not critical as long as it is greater than 10 msec.

Thus, as long as information is being received via the RS232 serial input from the commercial computer, the relay will remain closed (connected) and output from the interface board will be directed to the military communications link in the form of tones for possible broadcast over the GDU's radio.

The analog output generator element uses a 74164 8-bit parallel-out serial shift register. The cosinusoidal analog output is actually generated digitally in the form of a series of steps that approximate the desired waveform. Analog filtering using a low-pass filter smooths out the steps and generates an output that closely approximates a cosine function. An operational amplifier is used to form an analog sum. The circuit, shown in Figure 5 is similar to the design of a digital to analog converter.

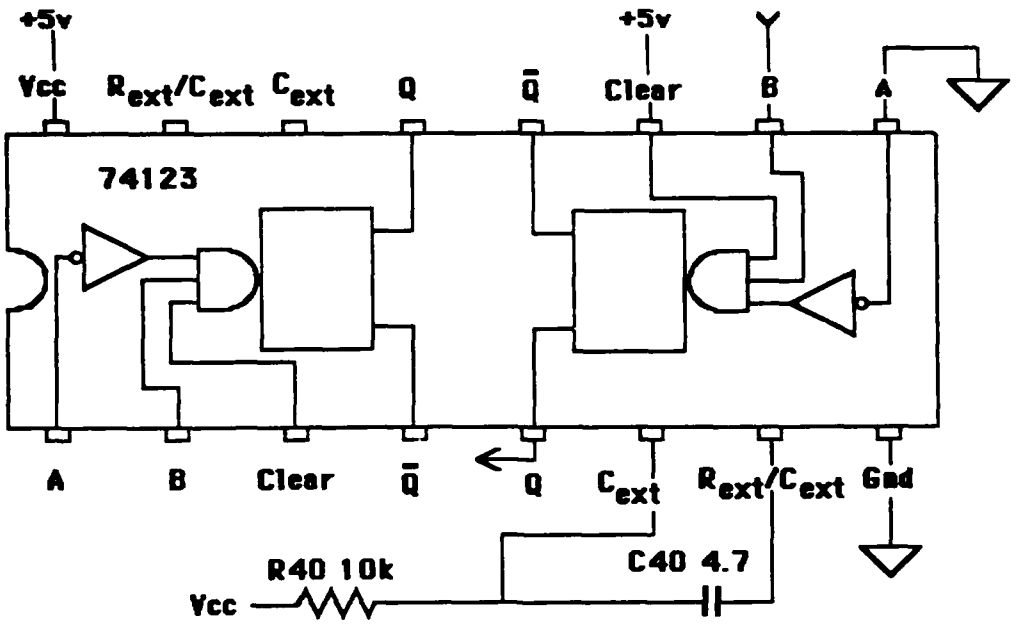

Figure 4. Retriggerable Monostable Multivibrator Element.

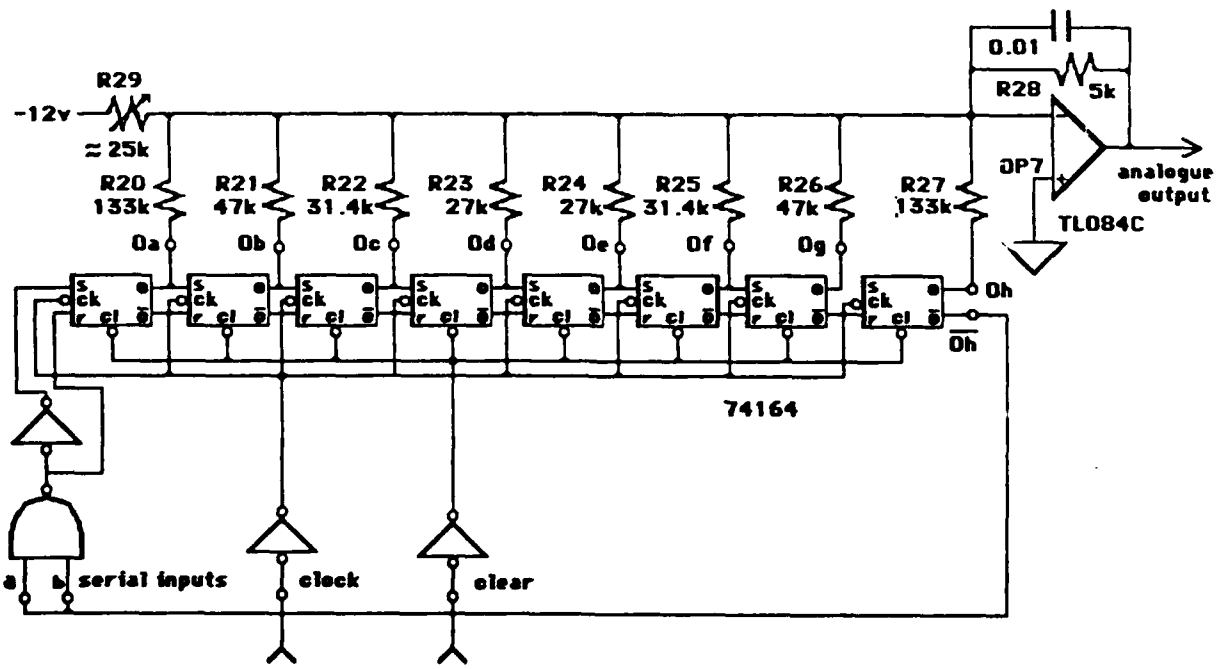

Figure 5. Analog Output Generator Element of the Modulator Section of the Interface Board.

The eight individual shift register units within the 74164 integrated circuit are denoted as Oa through Oh. In the modulator circuit the output from Oh is inverted logically and fed into the input of Oa. As a consequence, 16 separate clock pulses are required for the 8-bit shift register to complete a sequence. Upon being reset, Oa through Oh are all at logic level "zero" or "low." After one clock pulse, Oa becomes high. After two clock pulses, both Oa and Ob become high. After eight clock pulses, Oa through Oh are all high. On the ninth clock pulse Oa becomes zero but Ob through Oh are still high. On the sixteenth clock pulse all the outputs are again zero, thus completing the sequence.

Clocking occurs when a positive going pulse is applied to the "clock" input.

Each of the eight individual shift register units is connected to the inverting input of an operational amplifier, OP7, wired to form a summing unit. As can be seen, Oa is connected to the inverting input of OP7 by the resistor R20. Output from OP7, due to a voltage, Va, at the output of Oa is simply where

$$- Va * R28 / R20,$$

R28 is the value of the feedback resistor associated with OP7. Similar expressions exist for the other seven shift register sections of the 74164 8-bit parallel-out serial shift register.

By knowing the voltage pattern needed to form a cosine function composed of sixteen discrete steps, one may select values for R20 through R27, as well as R28 and R29 that will yield a good approximation. Normally, the eight outputs from the 74164 IC are either about 0.5 v or about 2.4 v, which correspond to "false" or "low" outputs or "true" or "high" outputs, respectively. The purpose of R29 is to remove any direct current (DC) bias in the output.

Upon being reset, the analog output generator has Oa through Oh set to "zero." Since there are 16 clock cycles for each cosine cycle of two pi radians, each clock pulse will advance the output 22.5 degrees in phase. Since the gain associated with each of the eight shift register outputs is inversely proportional to the corresponding effective resistance, the resistance value of the resistors associated with Oa through Od are computed as 13.14, 4.61, 3.08, and 2.61 ohms, respectively, where the values have been normalized to 1 ohm when all are connected in parallel. The resistance values associated with Oe through Oh are, by symmetry, 2.61, 3.08, 4.61, and 13.14 ohms, respectively. As can be seen from the schematic diagram of Figure 5, each of the above values have been multiplied by 10,000 in the circuit.

It is desirable to have the output of the analog output generator element to be zero when circuits Oa through Od only are in a positive or high logic level. These four at a high logic level with Oe through Oh in a low level state corresponds to a zero crossing of the output. This zero condition is achieved by adjusting R29 to approximately 25k ohms. This value may vary depending upon the particular 74164 used in the circuit. The output gain is adjusted (negatively) by the use of R20. It has been found that a nominal value of 1.5k ohms gives an output that matches the amplitudes normally encountered in radio communications systems.

5. CONCLUSIONS AND RESULTS

The purpose of the design and construction of the interface board was to support the Firepower Control Experiment of December 1985. The interface board was used many hours and during that time no known errors of conversion were ever detected, nor did the board suffer any known loses due to circuit construction practices.

Though the board performed satisfactorily in usage, the author does not want to leave the impression that the design is optimum for this particular use. Waddell, in 1986, used numerical modeling techniques to analyze the performance of the demodulator section in the presence of degraded input waveforms. His analysis yielded somewhat different resistor and capacitor values and an improved performance. Though his results have not been verified in actual hardware, interested users, that have similar requirements for an inexpensive interface board, should consult his results.

6. REFERENCES

Berlin, Howard M. Design of Active Filters, With Experiments. Howard W. Sams & Co., Inc., 1977.

Waddell, Scott V. A Numerical Simulation of a Telecommunications Circuit in Pascal. DoD Science and Engineering Apprenticeship Program, The George Washington University, Dr. Mark D. Kregel, Mentor, U.S. Army Ballistic Research Laboratory, 1987.

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